COLLEGE OF ENGINEERING & MANAGEMENT,

KOLAGHAT

ANALOG ELECTRONIC CIRCUITS LAB MANUAL

Subject Code: EC492

Dept Of Electronics & Communication Engineering

VISION

Pursuing Excellence in Teaching-Learning Process to Produce High Quality Electronics and Communication Engineering Professionals.

MISSION

To enhance the employability of our students by strengthening their creativity with different innovative ideas by imparting high quality technical and professional education with continuous performance improvement monitoring systems.

To carry out research through constant interaction with research organizations and industry.

Course objective: This course is designed for the 4 th semester UG students of ECE. This course is intended to develop an understanding of small signal amplifier design using linear transistor models; and its analysis at low and high frequencies, including different feedback topologies and oscillators. The course also indulges power amplifiers, tuned amplifiers and behavior of noise in an amplifier.

Program Educational Objectives (PEOs)

1	Attain a solid foundation in electronics & communication engineering fundamentals with an attitude to pursue continuing education and to succeed in industry / technical profession through global education.
2	Ability to function professionally in an increasingly international and rapidly changing world due to the advances in emerging technologies and concepts.
3	Exercise excellent leadership qualities on multi-disciplinary and multi-cultural teams, at levels appropriate to their experience, which addresses issues in a responsive, ethical, and innovative manner.
4	Contribute to the needs of the society in solving technical problems using electronics & communication engineering principles, tools, and practices.

Program Specific Outcomes (PSOs)

PSO-1 An ability to design and conduct the experiments, analyse and interpret the data using modern software or hardware tools with proper understanding (basic conceptions) of Electronics and Communication Engineering.

PSO-2 Ability to identify, formulate & solve problems and to apply the knowledge of electronics and communication to develop techno-commercial applications

PROGRAM OUTCOMES

PO1	**Engineering knowledge**	Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	**Problem analysis**	Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	**Design / development of solutions**	Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	**Conduct investigations of complex problems**	Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	**Modern tool usage**	Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	**The engineer and society**	Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	**Environment and sustainability**	Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	**Ethics**	Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	**Individual and team work**	Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	**Communication**	Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	**Project management and finance**	Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	**Life-long learning**	Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

COURSE OUTCOMES (COs)

Program Name: B. Tech in Electronics and Communication Engineering

SECOND YEAR: 4th SEMESTER		
Course Name (Code)	**Course Outcomes (COs)**	
	On completion of the course, the students will be able to:	
Analog Electronic Circuits Lab (EC492)	CO1	Design and test rectifiers, clipping circuits, clamping circuits and voltage regulators.
	CO2	Compute the parameters from the characteristics of JFET and MOSFET devices.
	CO3	Design, test and evaluate BJT amplifiers in CE configuration.
	CO4	Design and test JFET/MOSFET amplifiers.
	CO5	Design and test a power amplifier.
	CO6	Design and test various types of oscillators.

Mapping of COs with POs

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	P011	PO12
CO1	3	2	1	2	2	1	2	1	2	1	2	3
CO2	3	2	1	2	2	1	2	1	2	1	2	3
CO3	3	2	1	2	2	1	2	1	2	1	2	3
CO4	3	2	1	2	2	1	2	1	2	1	2	3
CO5	3	2	1	2	2	1	2	1	2	1	2	3
CO6	3	2	1	2	2	1	2	1	2	1	2	3
AVG.	3	2	2	2	2	1	2	1	2	1	2	3

CO – PSO Mapping

	PSO-1	PSO-2
CO1	3	3
CO2	3	3
CO3	3	3
CO4	3	3
CO5	3	3
CO6	3	3

SYLLABUS

Analog Electronic Circuits Lab

EC492

- Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative).
- Design and set up the following rectifiers with and without filters and to determine ripple factor and rectifier efficiency: (a) Full Wave Rectifier (b) Bridge Rectifier.
- Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain- bandwidth product from its frequency response.
- Set-up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency.
- Realize BJT Darlington Emitter follower with and without bootstrapping and determine the gain, input and output impedances.
- Conduct an experiment on Series Voltage Regulator using Zener diode and power transistor to determine line and load regulation characteristics.
- Design and set-up the following tuned oscillator circuits using BJT, and determine the frequency of oscillation.
  R-C Phase shift Oscillator/Wien Bridge Oscillator.
- Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.
- Design, setup and plot the frequency response of Common Source JFET/MOSFET amplifier and obtain the bandwidth.

1. OBJECTIVE (S):

1.1.
1.2.

2. THEORY:

3. CIRCUIT DIAGRAM:

4. APPARATUS & COMPONENTS USED:

4.1 Apparatus:

Sl. No.	Apparatus	Range	Qty.

4.2 Components:

Sl. No.	Components	Specifications	Qty.

5. PROCEDURES:

6. EXPERIMENTAL DATA:

7. DATA ANALYSIS:

8. PRECAUTIONARY MEASURE TO BE TAKEN:

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3	Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain- bandwidth product from its frequency response.	19
4	Set-up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency.	24
5	Realize BJT Darlington Emitter follower with and without bootstrapping and determine the gain, input and output impedances.	28
6	Conduct an experiment on Series Voltage Regulator using Zener diode and power transistor to determine line and load regulation characteristics.	33
7	Design and set-up the R-C Phase shift Oscillator/ Wien Bridge Oscillator circuit using BJT and determine the frequency of oscillation.	38
8	Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.	46
9	Design, setup and plot the frequency response of Common Source JFET amplifier and obtain the bandwidth.	51

Experiment no. 1

Title: Conduct experiment to test diode clipping (single/double ended) and clamping circuits (positive/negative).

1. OBJECTIVE (S):

1.1. To observe the waveforms of clipper circuits using

- Positive and Negative clipper
- Biased clipper
- Combination clipper

1.2. To observe the waveforms of the Positive and Negative clamping circuits.

2. THEORY:

2.1. Clipping Circuits:

The clippers have the ability to remove signal voltages above or below a specified level & hence change the wave shape of the I/P signal. Most of the clippers employ diodes & are known as diode clippers. Different type of clippers are-

Positive & Negative clipper: A circuit that removes +ve half-cycle of the signal is called +ve clipper. Sometimes, it is required to remove the –ve half cycle of the I/P signal, the only thing to be done is to reverse the polarity of the diode connected across load, such a clipper is known as a –ve clipper.

Biased clipper: A clipper used to remove a small portion of +ve or–ve half cycle of the signal voltage is called a biased clipper. A diode is employed in series with a battery of different volts depending upon the requirement.

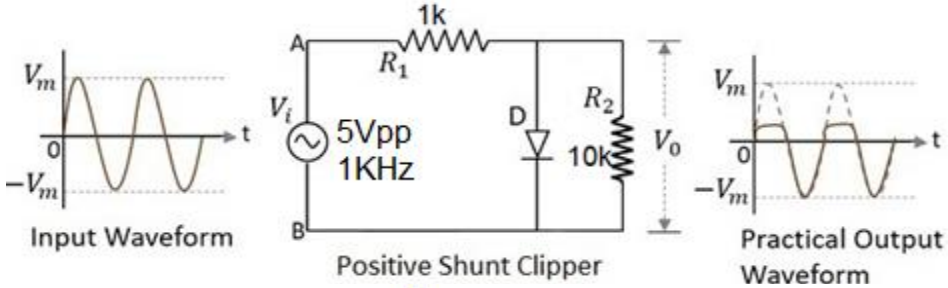
Combination clipper: In this circuit small portion of +ve as well as small portion of –ve half cycle of the signal voltage is removed.

2.2 Clamper:

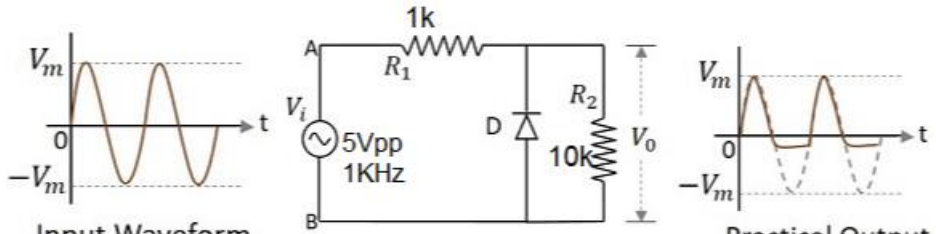
A clamping circuit adds d.c component to the signal in such a way that it pushes the signal either on the +ve side or on the –ve side. When the circuit pushes the signal on the +ve side then –ve peak of the signal falls on the zero level, this circuit is called a +ve clamper. When the circuit pushes the signal on the –ve side, this is –ve clamper.

3. CIRCUIT DIAGRAM:

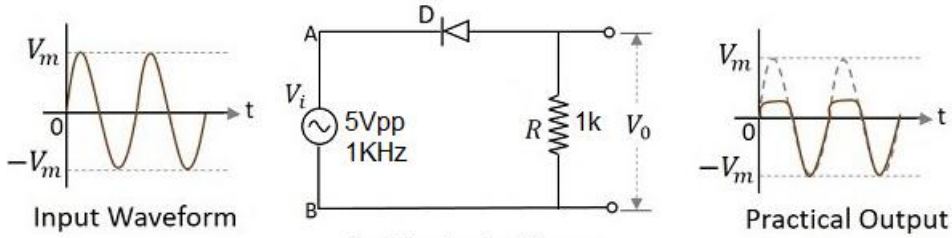
3.1. Clipping Circuits:



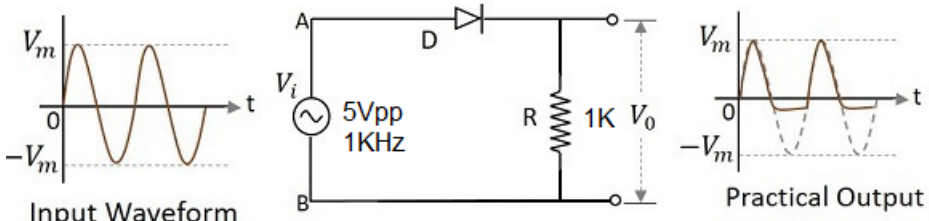
Input Waveform — Positive Shunt Clipper — Practical Output Waveform



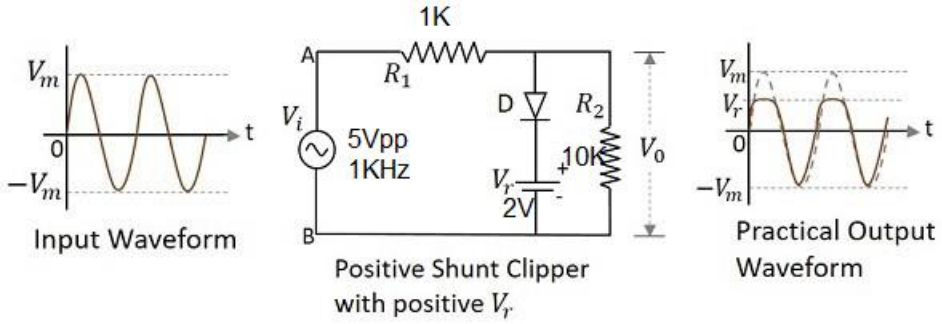
Input Waveform — Negative Shunt Clipper — Practical Output Waveform

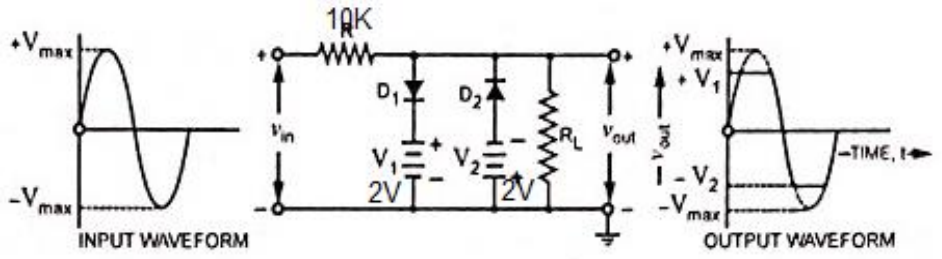


Input Waveform — Positive Series Clipper — Practical Output Waveform



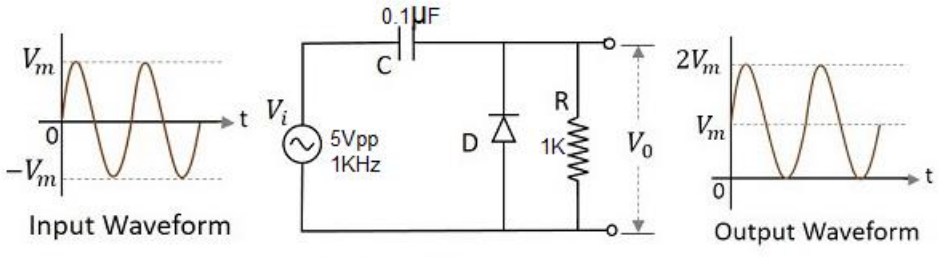
Input Waveform — Negative Series Clipper — Practical Output Waveform

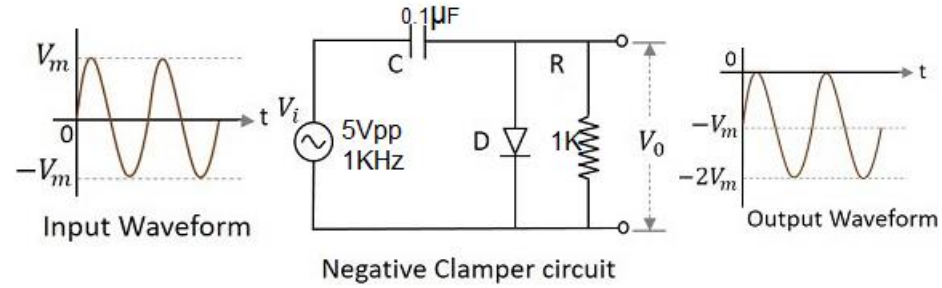




Combination Clipper

3.2. Clamping Circuits:





4. APPARATUS & COMPONENTS USED:

4.1 Apparatus:

Sl. No.	Apparatus	Range	Qty.
1	Trainer Kit	-	1
2	Multimeter	-	1
3	Function Generator	0 MHz to 10 MHz	1
4	DSO	0 MHz to 60 MHz	1

4.2. Components:

Sl. No.	Components	Specifications	Qty.
1	Resistors	1K,1/4 Watt	1
2	Resistors	10K ,1/4 Watt	1
3	Diode	1N4007	2
4	Capacitor	0.1µF	1

5. PROCEDURES:

Step-1: Connect the circuits as per the circuit diagram.
Step-2: Set input signal voltage (say5V, 1 kHz) using function generator.
Step-3: Observe the output waveform using DSO.
Step-4: Measure the amplitude and frequency of the output waveform from then DSO.
Step-5: Sketch the observed waveforms on the graph.

6. EXPERIMENTAL DATA:

Waveform:
Amplitude of the waveform:
Frequency of the waveform:

7. DATA ANALYSIS:

Sketch the observed waveforms on the graph paper.

8. PRECAUTIONARY MEASURE TO BE TAKEN:

1) Check the power supply terminals of the trainer kit.
2) Check the components to be used in the experiment.
3) Select proper mode of multimeter.
4) Connect the circuit carefully as per circuit diagram.
5) Don't give the power Supply without verifying the circuit by the class teacher.

9. SOME SAMPLE QUESTIONS:

i) What is meant by nonlinear wave shaping?
ii) What is clipper? What are the different types of clippers?
iii) What are the different applications of clipper?
iv) Explain the operation of positive and negative clipper?
v) What do mean by clamper?
vi) What are the different types of clamping circuits?
vii) What are the different applications of clampers?
viii) Explain the operation of positive clamper and negative clamper?

10. REFERENCE:

(A) Electronics Laboratory Primer – A Design approach by S. Poorna Chandra & B Sasikala.
(B) Linear Integrated Circuit by R.P. Jain & D. Roy Chowdhury.
(C) Operational Amplifier and Linear Integrated Circuit by Ramakant A. Gayakwad.

Experiment no. 2

Title: Design and set up the following rectifiers with and without filters and to determine ripple factor and rectifier efficiency: (a) Full Wave Rectifier (b)Bridge Rectifier

1. OBJECTIVE(S):

1.1. To determine ripple factor, regulation and efficiency of half-wave rectifier with & without filter.
1.2. To determine ripple factor, regulation and efficiency of full-wave rectifier with & without filter.
1.3. To determine ripple factor, regulation and efficiency of bridge rectifier with & without filter.

2. THEORY:

The process of converting an alternating current (or voltage) into a direct current (or voltage) is termed *Rectification*. Since the forward current of a p-n junction diode is much larger than the reverse current, it can be used as a rectifying device.

(i) Half-wave rectification of a semiconductor Diode

In the circuit of fig.1, the supply voltage is alternating. A large diode current will flow only during the positive half cycles of this voltage. As a result, the load voltage V_L will practically consists of half sinusoids and will posses a d.c component. Since the negative half cycles of the input signal are almost cut off and absent from the output signal.

In addition to the d.c component, the output voltage V_L of the rectifier will contain periodically fluctuating components, called *ripples*. Hence conversion of a.c to d.c by the rectifier is imperfect. The performance of the rectifier can be improved by inserting an additional circuitry between the rectifier & the load Resistance to reduce the ripples, called *Filter*.

$I_{dc}= 1/2\pi\int_0^{2\pi} I_m(sin\omega t)d\omega t=I_m/\pi$ Similarly

$V_{dc}= V_m/\pi$

$I_{rms} =\sqrt{1/2\pi \int_0^{2\pi} I_{ac}^2\, \omega t}$ $=I_m/2$ similarly

$V_{rms} = V_m/2$

Ripple facor ɤ $=V_{ac}/V_{dc} =1.21$(Theoretical)

Efficiency η $= P_{dc}/P_{ac} = \frac{0.406}{1+\frac{R_f}{R_L}} \simeq 40.6\%$

(ii) Full-wave rectification of a semiconductor Diode

If the rectified current passes through the load resistance in the same direction during the complete cycle of the input signal, the rectifier is said to be full-wave rectifier. The circuit is as shown in fig.2. Here two identical diodes and a centre tapped auto transformer is used. The two diodes conduct in alternate half cycle of the input voltage. The performance can be improved by inserting the filter. Using bridge rectifier circuit using four diodes as shown in fig.3 the full- wave rectification can be performed because the rectified current passes through the load at same direction.

$I_{dc}=1/2\pi[\int_0^{\pi} I_m \sin\omega t d\omega t - \int_{\pi}^{2\pi} I_m \sin\omega t d\omega t]=2I_m/\pi$

Similarly

$V_{dc}= 2V_m/\pi$

$I_{rms} = \sqrt{1/2\pi[\int_0^2 I_m^2 \sin^2 \omega t d\omega t}$ = $I_m/\sqrt{2}$ similarly

$V_{rms} = V_m/\sqrt{2}$

Ripple facor ϒ =Vac/Vdc = 0.48 (Theoretical)

Efficiency η = $P_{dc}/P_{ac} = \frac{0.81}{1+\frac{R_f}{R_L}} = 81.2\%$

Regulation:

The variation of the d.c output voltage as a function of d.c load current is known as regulation. The % Regulation is given by

% Regulation = $V_{NL}- V_L/V_L$ x100%

V_{NL} is the no load voltage.

3. CIRCUIT DIAGRAM:

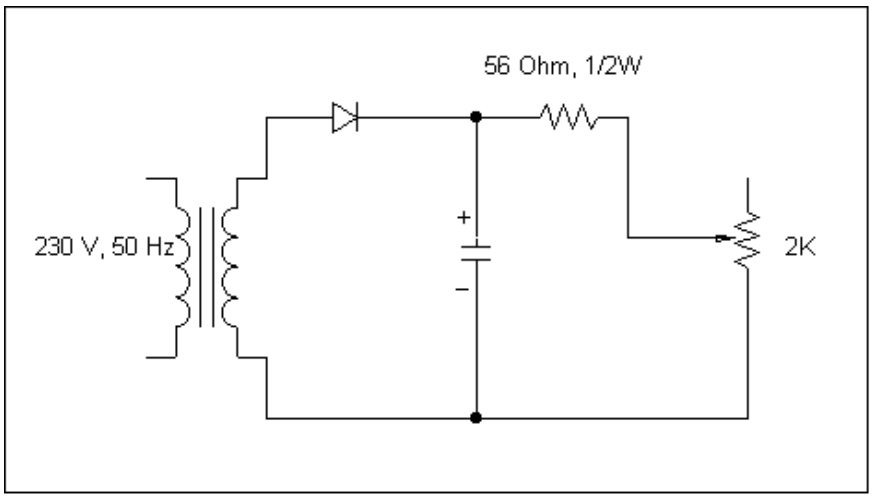


Fig.1Circuit For Half-Wave Rectifier

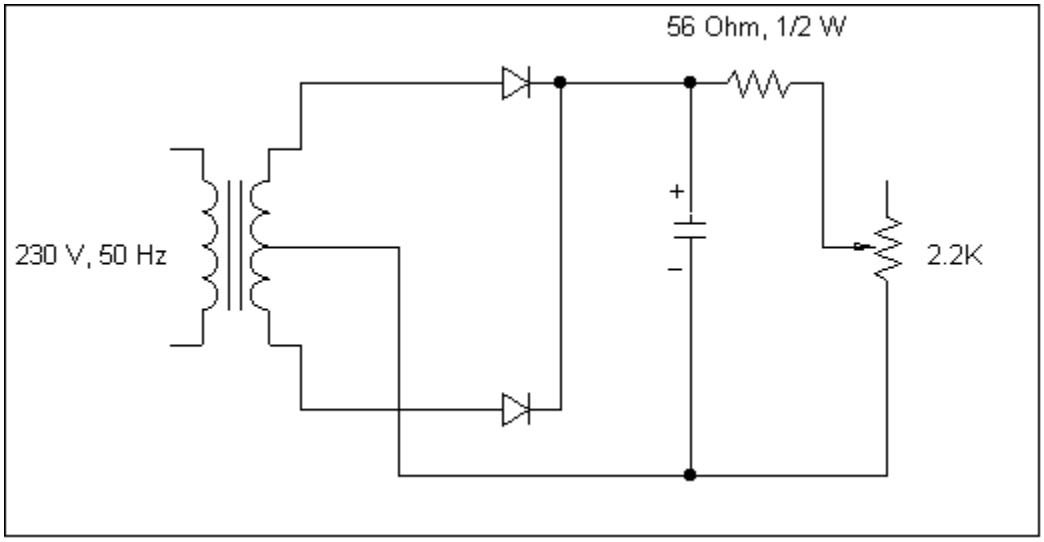


Fig.2 Circuit for Full-Wave Rectifier with CT Transformer.

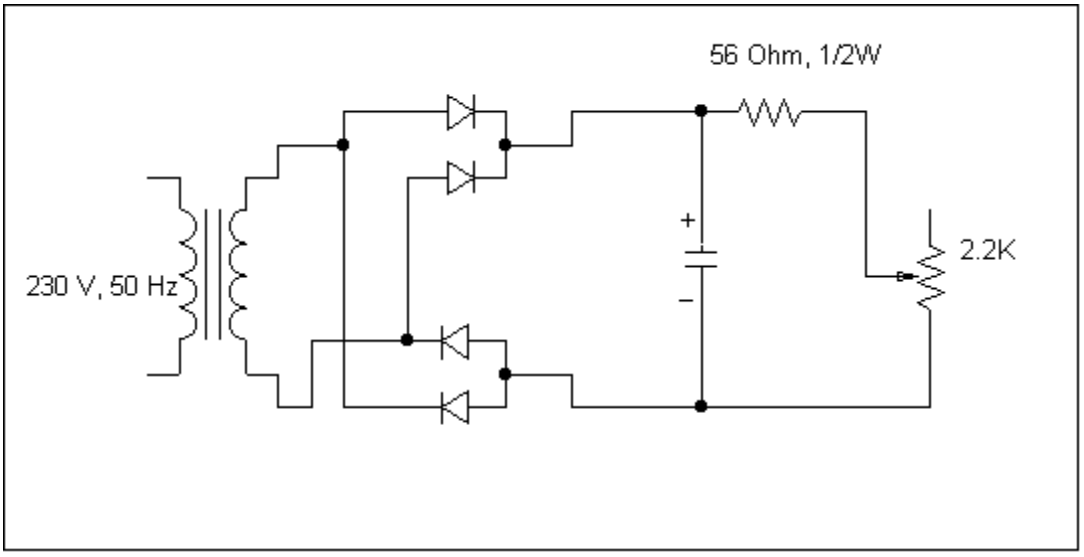


Fig.3 Circuit For Full-Wave Rectifier With Bridge Circuit

4. APPARATUS & COMPONENTS USED:

4.1. Apparatus:

Sl. No.	Apparatus	Range	Qty.
1	Trainer Kit	-	1
2	Multimeter	-	1
3	Function Generator	0 MHz to 10 MHz	1
4	DSO	0 MHz to 60 MHz	1

4.2. Components:

Sl. No.	Components	Specifications	Qty.
1	Resistors	56Ω,1/2 Watt	1
2	Pot	2KΩ, 2.2KΩ	1
3	Diode	1N4007	4
4	Capacitor	100μF/35V,1000μF/35V	1

5. PROCEDURES:

(i) To draw Regulation characteristic of a Half-wave rectifier

1. Construct the circuit as shown schematically in Fig.1. using 220V/12V transformer and with specified R_L.
2. Switch on the CRO and adjust the voltage and time scale as directed.
3. Measure the transformer secondary voltage V_S(rms value) by multimeter and observe the wave-form in CRO.
4. Measure No-Load voltage i.e the open circuit output dc voltage V_{NL}.
5. Set different values of load resistances by adjusting pot connected as load resistance & measure dc voltage (V_{Ldc}) across each load resistance and calculate corresponding load current keeping input voltage constant in each case.
6. Connect one smoothing capacitor across R_L. Repeat steps 4&5.
7. For a particular value of R_L measure the ac load voltage (V_{Lac}) using ac scale and also measure dc load voltage (V_{Ldc}).

For Full-wave rectifier Experimental procedures are same except circuit diagram.

6. EXPERIMENTAL DATA:

(a) Maximum forward current Rating:
(b) Maximum PIV:

Table1
Data for Regulation characteristic

No load Voltage V_{NL}=

Without Filter				With Filter			
load Resist. R_L(Ohm)	Load Volt. V_L(V)	Load Current I_L(mA)	% Reg. =V_{NL}-V_L/V_Lx100	load Resist. R_L(Ohm)	Load Volt. V_L(V)	Load Current I_L(mA)	% Reg. =V_{NL}-V_L/V_Lx100

Table2

Determination of ripple factor
Input voltage V_S=
Load resistance R_L=

Without Filter			With Filter		
dc load voltage(V_{Ldc})(V)	ac load voltage (V_{Lac})(V)	r.f= V_{Lac}/ V_{Ldc}	dc load voltage(V_{Ldc})(V)	ac load voltage (V_{Lac})(V)	r.f= V_{Lac}/ V_{Ldc}

Determination of efficiency

$\eta = P_{dc}/P_{ac} = \left[\frac{V_{dc}}{V_{rms}}\right]^2$

7. DATA ANALYSIS:

I. Plot the dc load current (along X-axis) Vs. the dc load voltage (along Y-axis). That curve is known as *Load Regulation Characteristic* of Half-wave Rectifier.
II. Calculate % Regulation as mentioned in data table.
III. Calculate ripple factor (r.f) as mentioned in data table.
IV. Calculate efficiency as mentioned.
For Half-wave, Full wave and Bridge rectifier.

8. PRECAUTIONARY MEASURE TO BE TAKEN:

1) Connect circuit properly & then only power on the circuit.
2) If any change of the circuit requires then power off first and then disassemble the circuit.
3) Check the capacitor polarity before power on of the circuit.

9. SOME SAMPLE QUESTIONS:

(i) What is rectification?
(ii) What is voltage regulation?
(iii) What is no-load voltage?
(iv) Define rectification efficiency.
(v) Define ripple factor.
(vi) Name an electronic device whose function is opposite to that of a rectifier.
(vii) What is bridge rectifier?
(viii) For an ideal regulator what is the value of percentage regulation?
(ix) What are the advantages of a bridge rectifier over a full-wave rectifier?

10. REFERENCE:

(A) Electronics Laboratory Primer – A Design approach by S. Poorna Chandra & B Sasikala.
(B) Linear Integrated Circuit by R.P. Jain & D. Roy Chowdhury.
(C) Operational Amplifier and Linear Integrated Circuit by Ramakant A. Gayakwad.

Experiment no. 3

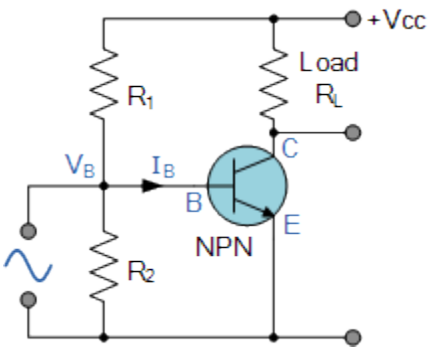
Title: Design and set up the BJT common emitter amplifier using voltage divider bias with and without feedback and determine the gain- bandwidth product from its frequency response.

1. OBJECTIVE (S):

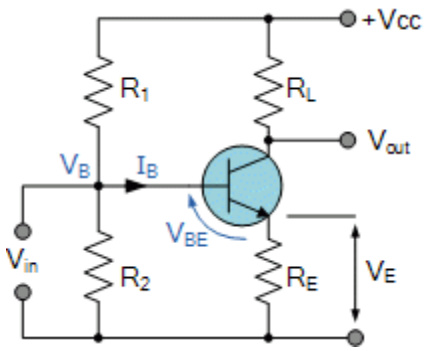
1.1. To design BJT common emitter amplifier using voltage divider bias with and without feedback.
1.2. To determine bandwidth, Mid band gain.

2. THEORY:

The common emitter configuration is widely used as a basic amplifier as it has both voltage and current amplification.
Resistors R1 and R2 form a voltage divider across the base of the transistor. The function of this network is to provide necessary bias condition and ensure that emitter-base junction is operating in the proper region.
In order to operate transistor as an amplifier, biasing is done in such a way that the operating point is in the active region. For an amplifier the Q-point is placed so that the load line is bisected. Therefore, in practical design V_{CE} is always set to $V_{CC}/2$. This will confirm that the Q-point always swings within the active region. This limitation can be explained by maximum signal handling capacity. For the maximum input signal, output is produced without any distortion and clipping.



Without feedback



With feedback

Design:

Given Transistor parameters:

V_{CEO} = 60 V, $I_{C\,max}$ = 100 mA

$V_E = 0.1\ V_{CC}$ (applying $1/10^{th}$ rule for design)

= 1.5 V (Since V_{CC} = 15V)

$$V_E = I_C R_E \text{ or } R_E = \frac{V_E}{I_C} = \frac{1.5}{0.1} = 15\ \Omega$$

Taking standard value $\mathbf{R_E = 27\ \Omega}$

$R_C = 4 \times R_E = 4 \times 27 = 108\ \Omega$

Taking standard value $\mathbf{R_C = 100\ \Omega}$

$I_{CQ}R_E = 0.1V_{CC}$

$$I_{CQ} = \frac{0.1 \times 15}{27} = 0.0555 \approx 0.056A$$

$V_1 = V_{BE} + I_{CQ}R_E$ (applying KVL)

$= 0.7 + 0.056 \times 27 = 2.212$ V

$I_1 = 0.1 \times I_{CQ} = 0.0056A$

$$R_1 = \frac{V_1}{I_1} = \frac{2.212}{0.0056} \approx 400\ \Omega$$

Taking standard value $\mathbf{R_1 = 470\ \Omega}$

$V_1 = Vcc - I_{CQ}R_2$

$$\mathbf{R_2} = \frac{Vcc - V_1}{I_{CQ}} = \frac{15 - 2.212}{0.056} = \mathbf{2.2\ K\ \Omega}$$

Calculation of bypass capacitor C_b:

For this capacitor audio frequency is taken , f = 20Hz

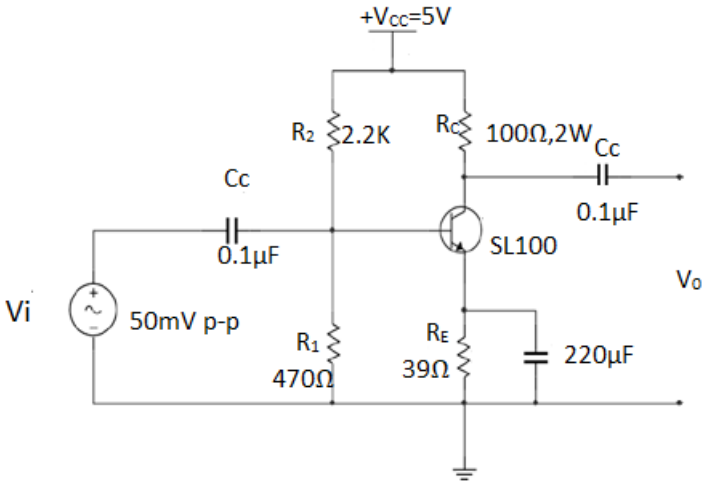
$$C_b = \frac{10}{2\pi f R_E} = \frac{10}{2 \times \pi \times 20 \times 27} \approx 220\ \mu F$$

$$Cc = \frac{10}{2\pi f R_b}$$

$$R_b = \frac{R_1R_2}{R_1 + R_2} = \frac{2.2 \times 0.47}{2.2 + 0.47} = \frac{1.034}{2.67} = 0.387\ K\Omega \approx 0.4\ K\Omega$$

$$Cc = \frac{10}{2 \times 3.14 \times 20 \times 0.4 \times 10^3} \approx 0.1\mu F$$

3. CIRCUIT DIAGRAM:



4. APPARATUS & COMPONENTS USED:

4.1 Apparatus:

Sl. No.	Apparatus	Range	Qty.
1	Trainer Kit	-	1
2	Multimeter	-	1
3	Function Generator	0 MHz to 10 MHz	1
4	DSO	0 MHz to 60 MHz	1

4.2 Components:

Sl. No.	Components	Specifications	Qty.
1	Resistors	39Ω,470Ω,2.2KΩ,1/4Watt	1
2	Resistors	100Ω, 2Watt	1
3	Transistor	SL100	2
4	Capacitor	0.1μF,220μF	1

5. PROCEDURES:

Step-1: Construct the circuit as per the circuit diagram.
Step-2: Set V_i = 50mV (say), using the signal generator.
Step-3: Keeping the input voltage constant, vary the frequency from 100 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
Step-4: For without feedback, Remove the R_E from the circuit and repeat the steps and observe the frequency response in the absence of R_E.

6. EXPERIMENTAL DATA:
(With or without feedback)

V_i = 50mV

Sl No.	Frequency	V_0 (volts)	Gain = V_0 / V_i	Gain (db) = 20 logV_0 / V_i

Result:
(With or without feedback)

Maximum Gain (A_{max}) =
3dB Gain =
3dB Lower cut-off frequency, f_L =
3dB Upper cut-off frequency, f_H =
3dB Bandwidth (f_H - f_L) =

7. DATA ANALYSIS:

I. Plot the graph gain *vs* frequency.
II. Calculate the bandwidth from the graph.

8. PRECAUTIONARY MEASURE TO BE TAKEN:

1) Check the power supply terminals of the trainer kit.
2) Check the components to be used in the experiment.
3) Select proper mode of multimeter.
4) Connect the circuit carefully as per circuit diagram.
5) Don't give the power Supply without verifying the circuit by the class teacher.

9. SOME SAMPLE QUESTIONS:

i) What are the applications of CE amplifier?
ii) What is cut off frequency? What is lower 3dB and upper 3dB cut off frequency?
iii) What is the equation for voltage gain?
iv) What is Bandwidth of an amplifier?
v) What is the importance of gain bandwidth product?

10. REFERENCE:

A) Electronics Laboratory Primer – A Design approach by S. Poorna Chandra & B Sasikala.
B) Linear Integrated Circuit by R.P. Jain & D. Roy Chowdhury.
C) Operational Amplifier and Linear Integrated Circuit by Ramakant A. Gayakwad.

Experiment no. 4

Title: Set-up and study the working of complementary symmetry class B push pull power amplifier and calculate the efficiency.

1. OBJECTIVE (S):

1.1 To design complementary symmetry class B push pull power amplifier.
1.2 To determine the efficiency of the amplifier.

2. THEORY:

The class B amplifier is biased at the Cutoff point so that Icq = 0 and Vceq =Vce(cut off). It is brought out of the cut off and operates in its linear region when input signal derives the transistor into conduction. The class B amplifier was developed to improve the low efficiency rating of class A Amplifiers. The maximum efficiency of class B amplifier has 78.5 %. As class B amplifier consumes less energy than class A but class B amplifier conducts only for 180°.

Class B Push Pull Operation

As class B amplifier only for positive half cycle to amplify the entire cycle. It is necessary to add second class B amplifier that operates on the negative half cycle. The combination is known as push pull operation.

Transformer Coupling

In this case the input is applied at transformer which has its center tap secondary grounded, producing phase inversion. It converts input signal into two out of phase signal for transistors. Transistor Q 1 will conduct on positive half cycle while Q2 will conduct for negative half cycle at negative half cycle when both transistors are NPN.

Complementary Symmetry Transistor

In this case one transistor is NPN while other is PNP. We used negative and positive power supplies. Class B Amplifier have cross over distortion problems. This distortion is caused by 0.7 volts which are used to turn on transistors. This problem can be solved by using class AB amplifier.

$P_O(ac) = V_L^2(ac)/2R_L$
$P_i(dc) = V_{CC}\, I_{dc}$
Efficiency $\eta = P_O(ac)/ P_i(dc)$

3. CIRCUIT DIAGRAM:

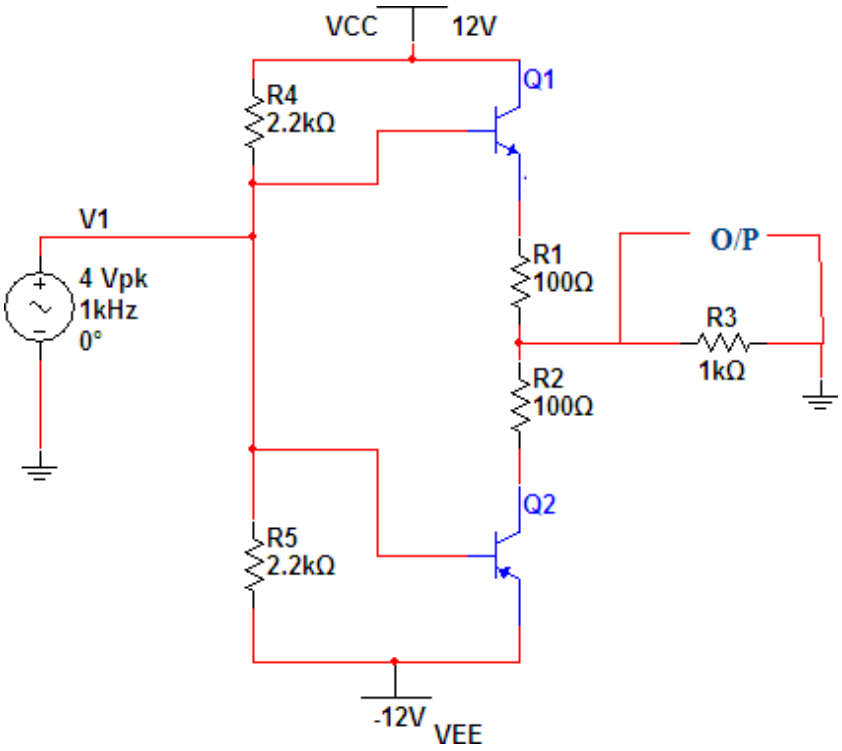


Fig.1

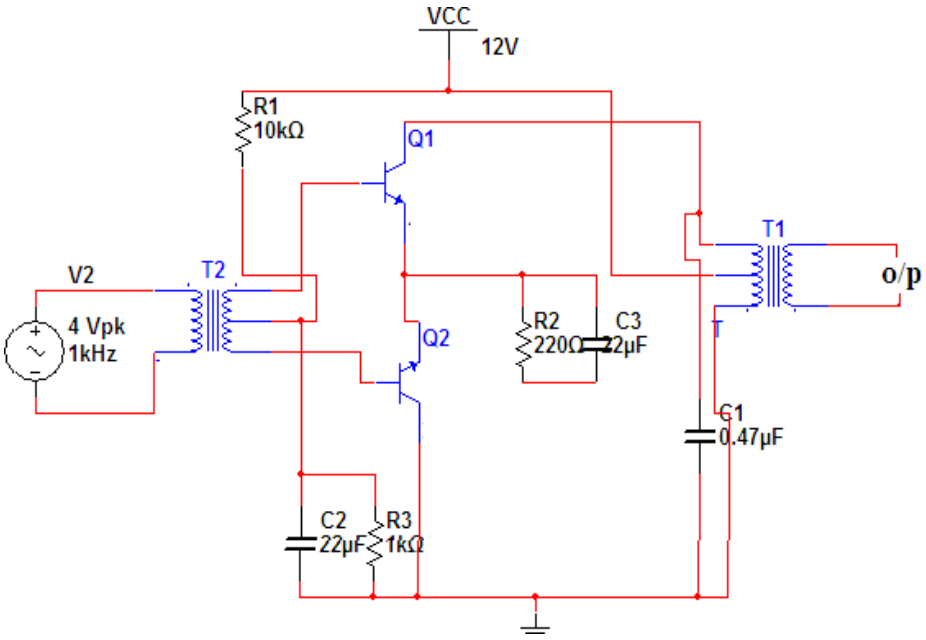


Fig.2

4. APPARATUS & COMPONENTS USED:

4.1 Apparatus:

Sl. No.	Apparatus	Range	Qty.
1	Trainer Kit	-	1
2	Multimeter	-	1
3	Function Generator	0 MHz to 10 MHz	1
4	DSO	0 MHz to 60 MHz	1

4.2 Components:

Sl. No.	Components	Specifications	Qty.
1	Resistors	100Ω,220Ω,1KΩ,2.2KΩ,10KΩ,1/4Watt	-
2	Transistor	CL100, CK100	-
3	Capacitor	22µF, 0.47µF	-
4	Transformer	-	-

5. PROCEDURES:

Step-1: Connect the circuit as per the circuit diagram of fig.1.
Step-2: Apply 4v p-p with 1KHZ frequency using function generator.
Step-3: Observe the waveforms in D.S.O and note the amplitude and time period of the input signal and output signal.
Step-4: Calculate the maximum output power and efficiency.

6. EXPERIMENTAL DATA:

7. DATA ANALYSIS:

8. PRECAUTIONARY MEASURE TO BE TAKEN:

1) Check the power supply terminals of the trainer kit.
2) Check the components to be used in the experiment.
3) Select proper mode of multimeter.
4) Connect the circuit carefully as per circuit diagram.
5) Don’t give the power Supply without verifying the circuit by the class teacher.

9. SOME SAMPLE QUESTIONS:

i) In class-B power amplifiers why crossover distortion will be occurred?
ii) what are the different methods to eliminate distortion?
iii) How much efficiency will be obtained in class-B power amplifier?
iv) Where is the location of operating point in class-B power amplifier?

10. REFERENCE:

(A) Electronics Laboratory Primer – A Design approach by S. Poorna Chandra & B Sasikala.
(B) Linear Integrated Circuit by R.P. Jain & D. Roy Chowdhury.
(C) Operational Amplifier and Linear Integrated Circuit by Ramakant A. Gayakwad.

Experiment no. 5

Title: Realize BJT Darlington Emitter follower with and without bootstrapping and determine the gain, input and output impedances.

1. OBJECTIVE (S):

1.1To design BJT Darlington emitter follower with and without bootstrapping.
1.2 To determine the Voltage gain, input impedance and output impedance.

2. THEORY:

Normally transistors are used as amplifiers. But there are some applications in which, matching of impedance is required between two circuits without any gain or attenuation. In such applications emitter followers are used. Sometimes, the current gain and input impedance of an emitter follower are insufficient to meet the requirement. Darlington emitter follower has two transistors connected in cascade such that the emitter of first transistor is connected to the base of second transistor. Therefore, the current gain of the pair is equal to product of individual current gain that is $\beta = \beta1*\beta2$.

DESIGN

Let V_{CE} = 6V, $I_{CQ} \approx I_{EQ}$=10mA (Q point of transistor Q2), ß=100 (SL 100)
Then $V_{CC} = 2V_{CE}$=2 x 6 =12 V
$I_E = I_C$ = 10 mA
$V_{R3} = V_{CC} – V_{CE}$= 12 – 6 = 6V
$R_E = V_{R3} / I_E$ = 6V / (10 mA) = 0.6K =560Ω (Choose)
$V_{R2} – V_{BE1} - V_{BE2} – V_{R3} = 0$
i.e , $V_{R2} = V_{BE1} + V_{BE2} + V_{R3}$
$= 0.6 + 0.6 + (I_E R_E) = 1.2 + (10x0.6) = 7.2V$
$V_{CC} = V_{R1} + V_{R2}$
$V_{R1} = V_{CC} – V_{R2}$ = 12 – 7.2 = 4.8 V
$I_{E1} = I_{B2} \approx I_{E2}$ / ß=10mA/ 100= 0.1mA
$I_{B1} = I_{E1}$ / hfe = 0.1mA / 100 = 1 µA
R1 = V_{R1}/ (10 (I_{B1})) = 4.8 / (10 x 1 µA) = 480 KΩ
R2 = V_{R2} / (9 I_{B1}) = 7.2 / (9 x 1 µA) = 800kΩ

To find Cc1

XcC1 ≤ Ri / 10 (Ri = R1|| R2 || hie = hie) Let fL=100Hz (Lower Cut-off Frequency)
fL= 1 / (2π*(Ri / 10)*Cc1)
Ri= R1 || R2 || hie
For the above darlington pair hie≈β_D*R_E
For SL100 β=150 and β_D= β* β=22500

Ri≈290 KΩ
So Cc1= 1 / 2π*(Ri/10)*fL= 1 / (2π*29KΩ*100) =0.05 uF
So, **Use Cc1 = 0.1μF or 0.47 μF**.

To find Cc2
Let fL=100Hz (Lower Cut-off frequency) ,RL=1KΩ
fL= 1 / 2π*(Ro+RL)*CE
But Ro=Re ≈ re Here, re=VT / Ic =26mV/10mA=2.6Ω
Re ≈ re ≈3Ω
1/(2π*fL* CE)= Re =>
Therefore,
CE=1/(2*π*100*(3+1KΩ)) CE =1.59 μF
Use Cc2 ≈0.47 or 2 μF

3. CIRCUIT DIAGRAM:

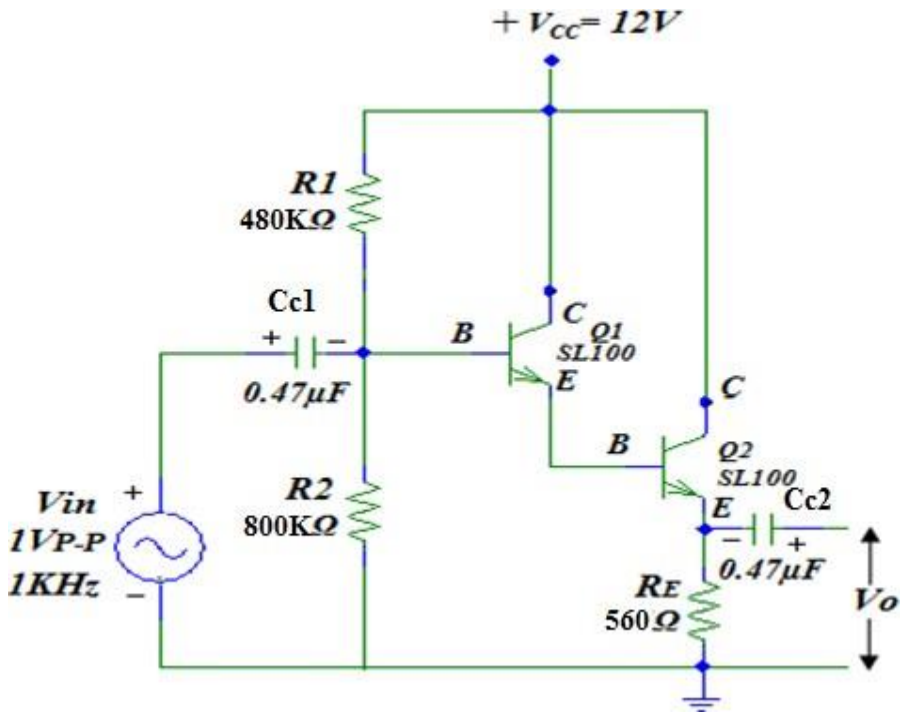


Fig.1 Darlington emitter follower without bootstrapping

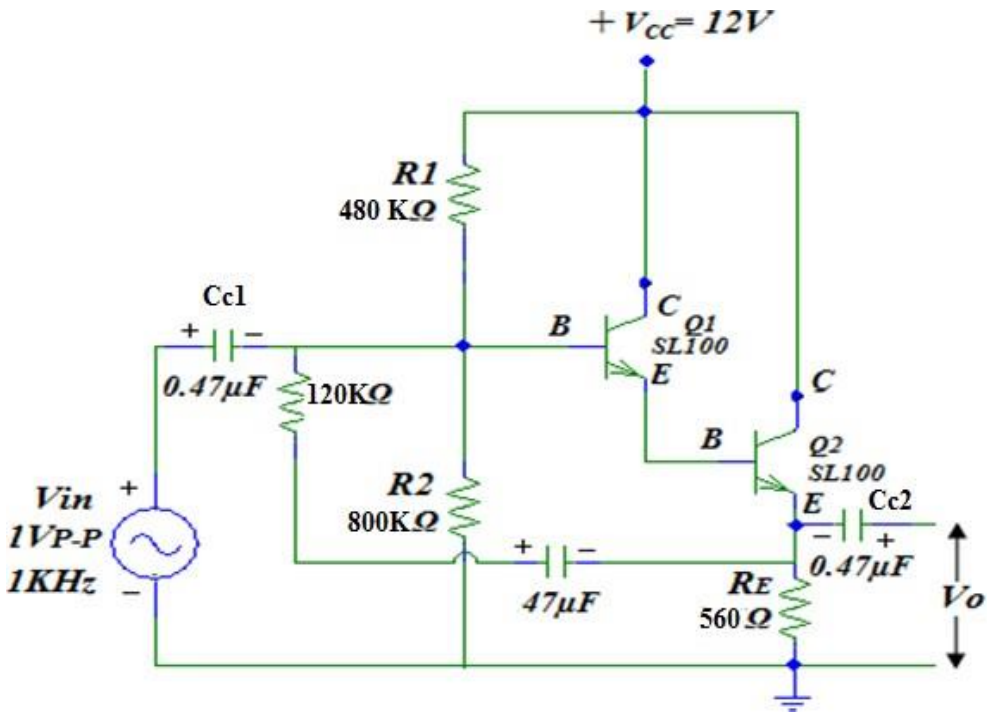


Fig.2 Darlington emitter follower with bootstrapping

4. APPARATUS & COMPONENTS USED:

4.1 Apparatus:

Sl. No.	Apparatus	Range	Qty.
1	Trainer Kit	-	1
2	Multimeter	-	1
3	Function Generator	0 MHz to 10 MHz	1
4	DSO	0 MHz to 60 MHz	1

4.2 Components:

Sl. No.	Components	Specifications	Qty.
1	Resistors	560Ω,120KΩ,480KΩ,800KΩ,1/4Watt	1
2	Transistor	SL100	2
3	Capacitor	0.47μF	2

5. PROCEDURES:

Step-1: Construct the circuit as per the circuit diagram of Fig 1.
Step-2: Set input signal voltage 50mV(p-p), 1 kHz using function generator.
Step-3: Keeping the input voltage constant, vary the frequency from 100 Hz to 1 MHz in regular steps and note down the corresponding output voltage.
Step-4: Repeat the procedure for circuit diagram in Fig 2. (With bootstrapping)

6. EXPERIMENTAL DATA:

$V_i = 50mV$

Sl No.	Frequency	V_0 (volts)	Gain = V_0 / V_i	Gain (db) = 20 logV_0 / V_i

Result:

	Theoretical	Practical
Input impedance		
Output impedance		
Gain (Mid band)		
Bandwidth		

7. DATA ANALYSIS:

I. Plot the graph gain *vs* frequency.
II. Find the input and output impedance:
III. $$Z_i = \frac{V_i R_s}{V_s + V_i}$$

IV. $$Z_0 = \frac{V_{load} - V_{no\text{ - }load}}{V_{load}} \times 100\%$$

V. Calculate the bandwidth from the graph.

8. PRECAUTIONARY MEASURE TO BE TAKEN:

1) Check the power supply terminals of the trainer kit.
2) Check the components to be used in the experiment.
3) Select proper mode of multimeter.
4) Connect the circuit carefully as per circuit diagram.
5) Don't give the power Supply without verifying the circuit by the class teacher.

9. SOME SAMPLE QUESTIONS:

i) What is Darlington emitter follower?
ii) Why do you call it as Darlington emitter follower?
iii) What is the difference between with and without bootstrapping?
iv) Benefits of with and without bootstrapping?
v) What is the difference between Darlington emitter follower and FET amplifier?
vi) Mention the application of emitter follower.

10. REFERENCE:

(A) Electronics Laboratory Primer – A Design approach by S. Poorna Chandra & B Sasikala.
(B) Linear Integrated Circuit by R.P. Jain & D. Roy Chowdhury.
(C) Operational Amplifier and Linear Integrated Circuit by Ramakant A. Gayakwad.

Experiment no. 6

Title: Conduct an experiment on Series Voltage Regulator using Zener diode and power transistor to determine line and load regulation characteristics.

1. OBJECTIVE (S):

1.1 To design and set up a transistor series regulator.
1.2 To plot Load current vs output voltage.
1.3 To plot Input voltage vs output voltage for a constant load current.

2. THEORY:

An ideal power supply maintains a constant voltage at its output terminals, no matter what current is drawn from it. The output voltage of a practical power supply changes with load current, generally dropping as load current increases. The power supply specifications include a full load current rating, which is the maximum current that can be drawn from the supply. The terminal voltage when full load current is drawn is called the full load voltage (V_{FL}). The no load voltage (V_{NL}) is the terminal voltage when zero current is drawn from the supply, that is, the open circuit terminal voltage.

One measure of power supply performance, in terms of how well the power supply is able to maintain a constant voltage between no load and full load conditions, is called its percentage voltage regulation.

An unregulated power supply has poor regulation, ie. output voltage changes with load variations. If a power supply has poor regulation, it possesses high internal impedance. A simple emitter follower regulator is shown in Fig.1. It is also called a series regulator since the control element (transistor) is in series with the load. It is also called as the pass transistor because it conducts or passes all the load current through the regulator. It is usually a power transistor. The zener diode provides the voltage reference, and the base to emitter voltage ofthe transistor is the control voltage.

The value of R_S must be sufficiently small, to keep the zener in its reverse breakdown region. Writing Kirchoff's voltage law to the output circuit,

$$V_O + V_{BE} - V_Z = 0$$

$$ie\ V_{BE} = V_Z - V_O$$

If V_Z is perfectly constant, the above equation is valid at all times, and any change in V_O must cause change in V_{BE}, in order to maintain equality.

When current demand is increased by decreasing R_L, V_O tends to decrease. From the above equation, it is seen that as V_Z is fixed, decrease in V_O increases in V_{BE}. This will increase the forward bias of the transistor, thereby increasing level of conduction. Thus, the output current is increased to keep $I_L R_L$ a constant. The reverse process occurs when R_L is increased. Thus, the above circuit keeps the output voltage constant, even if the load varies widely.

DESIGN

Output Voltage, V_O = 5 volts (regulated)
Output Current, I_L = 0 - 30 mA
Input Voltage, V_i = 10-15 V

Maximum power dissipated in the transistor = $(V_{imax} - V_O)\ I_{max}$

Select a transistor whose P_{dmax} is greater than the power dissipation calculated above and whose V_{CEO} is greater than $(V_{imax} - V_O)$.

Calculate base current $I_B = I_{max} / h_{FE.min}$.

Select a zener having breakdown voltage equal to

$V_Z = (V_O + 0.6)$ volts
$V_Z = 5 + 0.6 = 5.6$ V

Referring datasheet for zener diodes, power dissipation of the zener diode is found. The wattage rating of the zener = $V_Z I_{Zmax}$

Select zener diode of 5.6 V, 400mW

Input = 10 – 15 V Output = 0 - 30 mA at 5V
I_B = 30mA / 50 = 0.6 mA
I_{Zmax} = 400 mW / 5.6 V = 71.4 mA
I_{Zmin} = 10% of I_{Zmax} = 7.14 mA

$$R_{max} = \frac{V_{imin} - V_z}{I_{zmin} + I_B} = \frac{10 - 5.6}{(7{,}14 - 0.6) \times 10^{-3}} = 673\Omega$$

$$R_{min} = \frac{V_{imax} - V_z}{I_{zmax}} = \frac{15 - 5.6}{71.4 \times 10^{-3}} = 132\Omega$$

Select R = average of R_{min} and R_{max} = 330 Ω

Power rating of R is to be fixed considering maximum I^2R loss.

$$\text{Power loss, } I^2R = \left(\frac{V_{imax} - V_z}{R}\right)^2 \times R = \frac{15 - 5.6}{330} = 0.27\text{W}$$

Select R as 330 Ω, 0.5 W

3. CIRCUIT DIAGRAM:

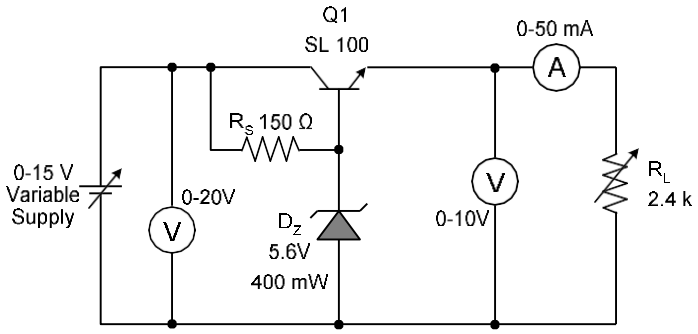


Fig.1 Circuit diagram of series regulator

4. APPARATUS & COMPONENTS USED:

4.1. Apparatus:

Sl. No.	Apparatus	Range	Qty.
1	Trainer Kit	-	1
2	Multimeter	-	1
3	Ammeter	0-50mA	1

4.2. Components:

Sl. No.	Components	Specifications	Qty.
1	Resistors	150Ω,1/4Watt	1
2	Zener diode	5.6V, 400mW	1
3	Transistor	SL100	1
4	POT	5KΩ	1

5. PROCEDURES:

(i) Load regulation

1. The circuit is wired as per the circuit diagram shown in fig. 1.
2. Keep the input voltage constant at V_{imin} , ie 10 V.
3. Vary the load resistance. Note *IL* and *VO* for each setting of *RL*. Ensure that *Vi* remains same throughout.
4. Draw a plot between *IL* and *VO*.

(i) Line regulation

Percent line regulation is another measure of the ability of a power supply to maintaina constant output voltage. In this case, it is a measure of how sensitive the output is to the changes in input or line voltage rather than to the changes in load. The specification is usually expressed as the percent change in output voltage that occurs per volt change in input voltage, with the load R_L assumed constant.

1. The circuit diagram is wired as per the circuit diagram shown in fig. 1.
2. Keep the load resistance R_L a constant.
3. Vary the input voltage between the limits for which the regulator is designed (10 to15V).
4. Note the load voltage *VO* for each setting of *Vin.*
5. Draw a graph between *Vin* (X axis) and V_L (Y axis).

6. EXPERIMENTAL DATA:

Load regulation

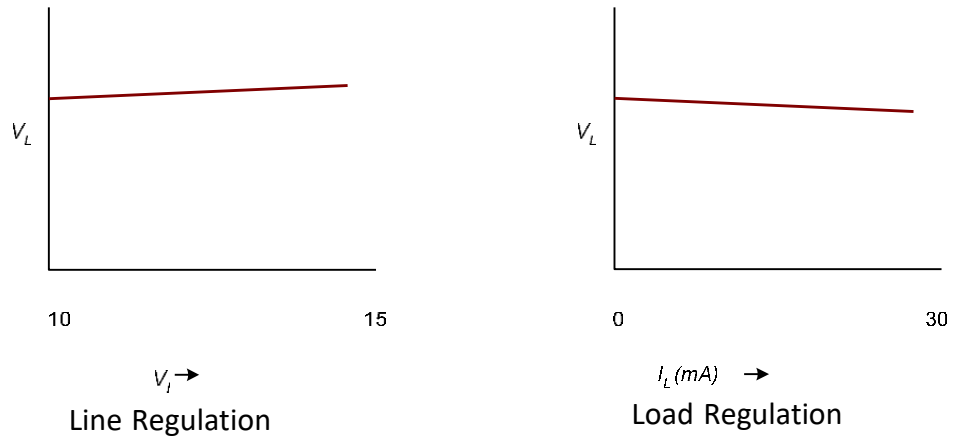
Load Current I_L mA	Output voltage V_O V

Line regulation

Input Voltage V_i V	Output voltage V_O V

7. DATA ANALYSIS:

EXPECTED OUTPUT PLOTS



Line Regulation

Load Regulation

8. PRECAUTIONARY MEASURE TO BE TAKEN:

1) Connect circuit properly & then only power on the circuit.
2) If any change of the circuit requires then power off first and then disassemble the circuit.

9. SOME SAMPLE QUESTIONS:

(i) Define percentage line and load regulation, what are the typical values?
(ii) What are the demerits of a series voltage regulator? How can they be avoided?
(iii) What is an SMPS? Where is it used?

10. REFERENCE:

(A) Electronics Laboratory Primer – A Design approach by S. Poorna Chandra & B Sasikala.
(B) Linear Integrated Circuit by R.P. Jain & D. Roy Chowdhury.
(C) Operational Amplifier and Linear Integrated Circuit by Ramakant A. Gayakwad

Experiment no. 7

Title: Design and set-up the R-C Phase shift oscillator/ Wien Bridge Oscillator circuit using BJT and determine the frequency of oscillation.

1.A: R-C Phase shift oscillator circuit using BJT

1. OBJECTIVE (S):

1.1. To design and construct RC phase shift oscillator.
1.2. Obtain a sinusoidal output and verify the practical frequency with calculated theoretical frequency.

2. THEORY:

The circuit arrangement of a phase shift oscillator using NPN transistor in CE configuration consists of voltage divider R1- R2 which provide the necessary bias, RE and CE combinations provide temperature stability and collector resistor RC controls thecollector voltage. The oscillator output voltage is coactively coupled to the load by CC.
In case of a transistor phase shift oscillator, the output of the feedback network is loaded appreciably by the relatively small input resistance (h_{ie}) of the transistor. Hence instead of employing voltage series feedback, voltage shunt feedback is used for a transistor phase shift oscillator. In this circuit, the feedback signal is coupled through the feedback resistor R' in series with the amplifier stage input resistance h_{ie}. The value of R' should be such that when added with the amplifier stage input resistance h_{ie} it is equal to R i.e., $R' + h_{ie} = R$.
The circuit is set in to oscillations by any random or variation caused in the base current, that may be due to noise inherent in the transistor or minor variation in voltage ofDC power supply. This variation in base current is amplified in collector circuit. The output of the amplifier is supplied to an RC feedback network. The RC network producesa phase shift of 180□ between output and input voltages. Since CE amplifier produces a phase reversal of the input signal, total phase shift becomes 360° or 0° which is essential for regeneration or for sustained oscillations. The output of this network is same as the originally assumed input to the amplifier and is applied to the base terminal of the transistor. Thus, sustained variation in collector current between saturation and cutoff values are obtained .RC phase shift network is the frequency determining network.

Design

Phase Shift Oscillator

$F = 1/ (2 \pi RC \sqrt{(6+4 (R_C/R))})$

R= 10 KΩ R_C =3.3 KΩ F=5 KHz

$5 \times 10^3 = 1/ (2 \pi 10 \times 10^3 \times C \times \sqrt{(6+(4 \times (3.3 \times 10^3 / 10 \times 10^3))))}$

$C = 0.001 \mu F V_{CE} < V_{CC} / 2 V_{CE} < 10 / 2$

$V_{CE} = 4V$

Kirchhoff's Voltage law for output circuit: $V_{CC} - V_{CE} = I_C R_C + I_E R_E$

$I_C \approx I_E = 2$ mA

$10 - 4 - I_C(R_C + R_E) = 0$

$R_C + R_E = 6 \times 10^3 / 2$

$R_E = 1$ KΩ

To find R_1 and R_2 :

$V_B = V_{CC} R_2 /(R_1 + R_2)$ (1)

Also $V_B = V_{BE} + V_E$

$V_B = 0.7 + 2 = 2.7$ For Silicon Transistor V_{BE} =0.7

From equation (1)

$2.7/10 = R_2 /(R_1 + R_2)$ (2)

$S= 1 + (R_B / R_E)$ (S= 10)

$R_B = 9$ KΩ

$R_B = R_1 R_2 / (R_1 + R_2)$ (3)

Substituting (2) in (3)

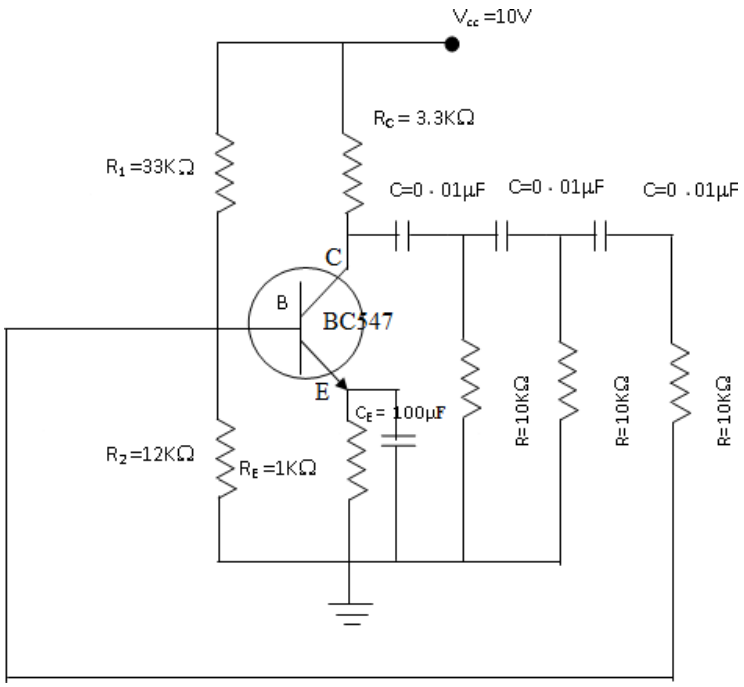
$9 = R_1 (0.27)$

$R_1 = 33$ KΩ

$R_2 = 12$KΩ

$C_E = 100$ μF

3. CIRCUIT DIAGRAM:



4. APPARATUS & COMPONENTS USED:

4.1 Apparatus:

Sl. No.	Apparatus	Range	Qty.
1	Trainer Kit	-	1
2	Multimeter	-	1
3	Function Generator	0 MHz to 10 MHz	1
4	DSO	0 MHz to 60 MHz	1

4.2 Components:

Sl. No.	Components	Specifications	Qty.
1	Resistors	1KΩ,3.3KΩ,12KΩ,33KΩ,10KΩ, 1/4 Watt	
2	Transistor	BC547	
3	Capacitor	0.01μF,100 μF	

5 PROCEDURES:

Step-1: Connections are made as per circuit diagram.

Step-2: Collector voltage signal is monitored in the DSO.

Step-3: The frequency is calculated from the waveform obtained.

Step-4: Base voltage signal is monitored in the DSO to check for the phase shift

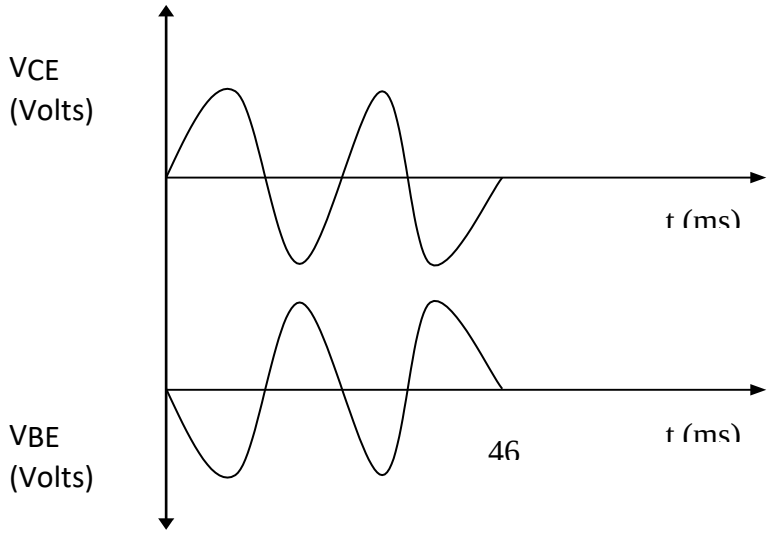
Step-5: The graphs are plotted for V_{CE} Vs Time and V_{BE} Vs Time.

6 EXPERIMENTAL DATA:

Amplitude Voltage (Vpp) Volts	Time Period (ms)	Theoretical frequency (Hz)	Practical frequency (Hz)

T =

f = 1 / T =



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7. DATA ANALYSIS:

Thus, the RC Phase shift oscillator is designed and its oscillations are Obtained.

8. PRECAUTIONARY MEASURE TO BE TAKEN:

1) Check the power supply terminals of the trainer kit.
2) Check the components to be used in the experiment.
3) Select proper mode of multimeter.
4) Connect the circuit carefully as per circuit diagram.
5) Don't give the power Supply without verifying the circuit by the class teacher.

9. SOME SAMPLE QUESTIONS:

(i) What is the basic principle of RC oscillators?
(ii) Why RC oscillators cannot generate high frequency oscillations?
(iii) Why we need a phase shift between input and output signal?
(iv) How is phase angle determined in RC phase shift oscillator?
(v) What is the drawback of phase shift oscillators?

10. REFERENCE:

(A) Electronics Laboratory Primer – A Design approach by S. Poorna Chandra & B Sasikala.
(B) Linear Integrated Circuit by R.P. Jain & D. Roychowdhury.
(C) Operational Amplifier and Linear Integrated Circuit by Ramakant A. Gayakwad.

1.B: Wien Bridge Oscillator circuit using BJT

1. OBJECTIVE (S):

1.1. To design and construct Wien bridge oscillator.
1.2. To observe the sinusoidal output waveform.

2. THEORY:

An oscillator is an electronic circuit for generating an AC signal voltage with a DC supply as the only input requirement. The frequency of the generated signal is decided by the circuit elements used. An oscillator requires an amplifier, a frequency selective network and a positive feedback from the output to the input. The Barkhausen criterion for sustained oscillation is Aβ = 1 where A is the gain of the amplifier and β is the feedback factor (gain). The unity gain means signal is in phase. (If the signal is 180^0 out of phase and gain will be -1).

A Wien bridge oscillator is a type of electronic oscillator that generates sine waves. It can generate a large range of frequencies. The oscillator is based on a bridge circuit originally developed by Max Wien in 1891 for the measurement of impedances. The bridge comprises four resistors and two capacitors. The oscillator can also be viewed as a positive gain amplifier combined with a bandpass filter that provides positive feedback. Automatic gain control, intentional non-linearity and incidental non-linearity limit the output amplitude in various implementations of the oscillator.

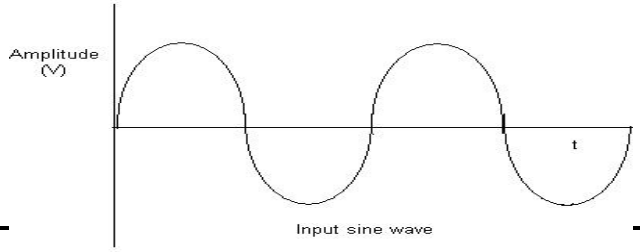
The circuit shown to the right depicts a common implementation of the oscillator, with automatic gain control, using modern components. Under the condition that $R_1=R_2=R$ and $C_1=C_2=C$, the frequency of oscillation is given by:

$$f = \frac{1}{2\pi RC}$$

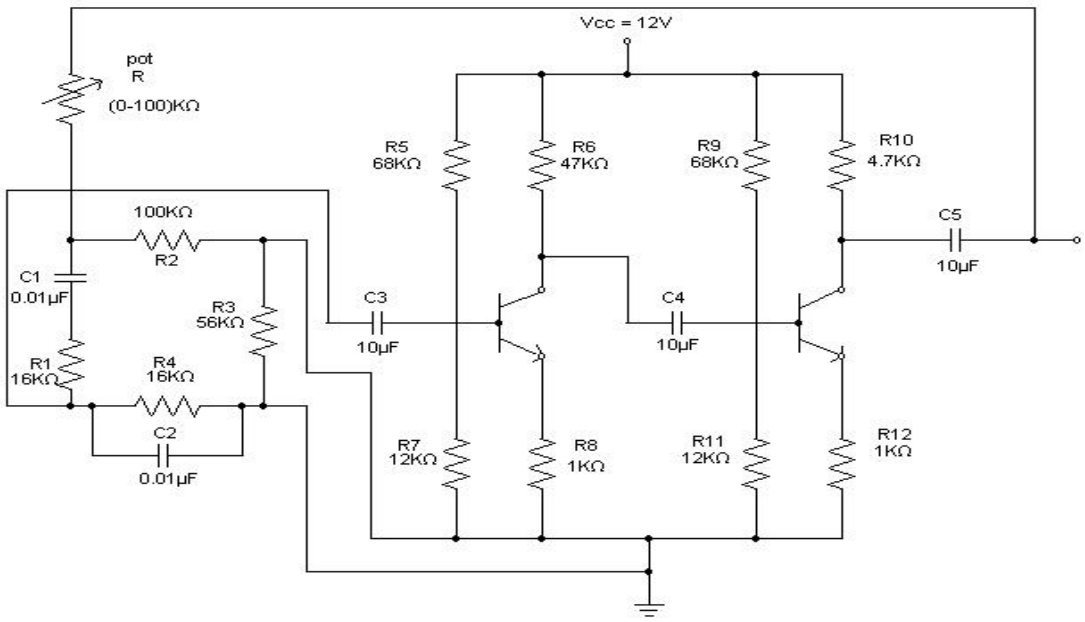
and the condition of stable oscillation is given by

$$R_b = \frac{R_f}{2}$$

MODEL GRAPH:



3. CIRCUIT DIAGRAM:



4. APPARATUS & COMPONENTS USED:

4.1 Apparatus:

Sl. No.	Apparatus	Range	Qty.
1	Trainer Kit	-	1
2	Multimeter	-	1
3	Function Generator	0 MHz to 10 MHz	1
4	DSO	1 MHz to 60 MHz	1

4.2 Components:

Sl. No.	Components	Specifications	Qty.
1	Resistors	1KΩ,4.7KΩ,12KΩ,16KΩ,47KΩ,56KΩ,68KΩ,100KΩ, 1/4 Watt	
2	Transistor	BC547	
3	Capacitor	0.01μF,10 μF	
4	POT	100KΩ	

5. PROCEDURES:

Step-1: Identify the pin details of BC107 Transistor (or equivalent silicon Transistor such as BC108/547) and test it using a multimeter. Set up the circuit on breadboard as shown in figure.

Step-2: A 12V Supply Voltage is given by using Regulated power supply and output is taken fromcollector of the Transistor.

Step-3: By using CRO the output time period and voltage are noted.

Step-4: Plot all the readings curves on a single graph sheet.

6. EXPERIMENTAL DATA:

Sl No	Amplitude(volts)	Time(ms)	Frequency

7. DATA ANALYSIS:

Thus, the Wein Bridge oscillator using Transistor was obtained and theoutput waveform was plotted.

8. PRECAUTIONARY MEASURE TO BE TAKEN:

1) Check the power supply terminals of the trainer kit.
2) Check the components to be used in the experiment.
3) Select proper mode of multimeter.
4) Connect the circuit carefully as per circuit diagram.
5) Don't give the power Supply without verifying the circuit by the class teacher.

Experiment no. 8

Title: Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.

1. OBJECTIVE (S):

1.1. To plot the drain characteristic.
1.2. To plot the transfer characteristic.
1.3. Determination of drain resistance, mutual conductance and amplification factor.

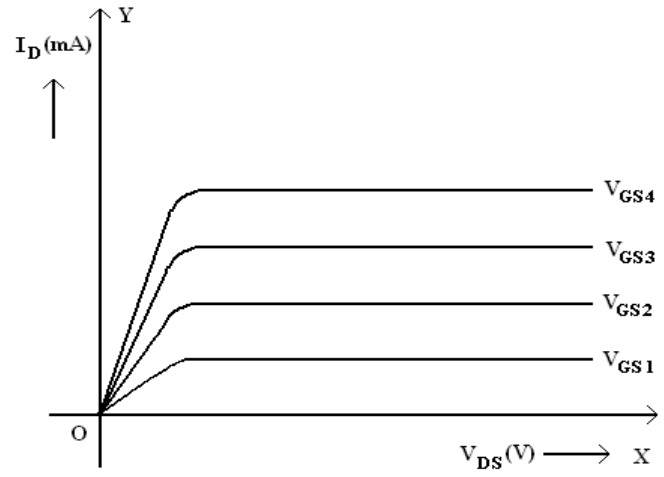
2. THEORY:

FORMULA USED:
1. Trans conductance $g_m = \Delta I_D / \Delta V_{DS}$ mho
2. Output resistance $r_{DS} = \Delta V_{DS} / \Delta I_D$ ohm

Where:
ΔI_D = Change in drain current.
ΔV_{DS} = Change in drain to source voltage

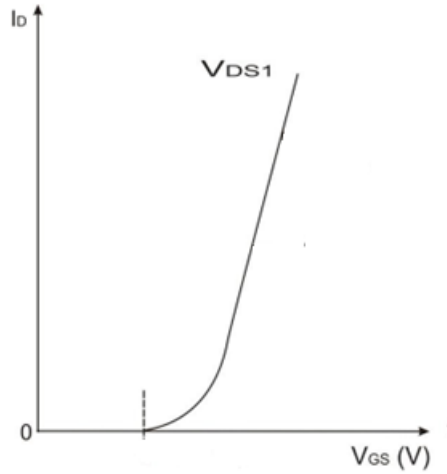
Drain Characteristics:

Model Graph:

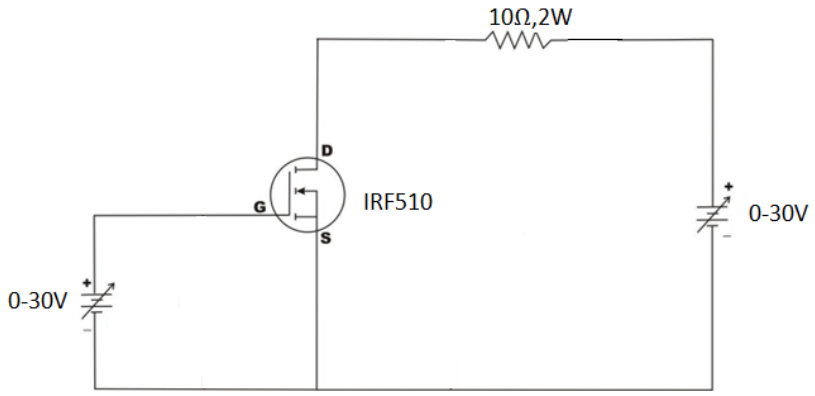


Transfer Characteristics:

Model Graph:



3. CIRCUIT DIAGRAM:



4. APPARATUS & COMPONENTS USED:

4.1 Apparatus:

Sl. No.	Apparatus	Range	Qty.
1	Trainer Kit	-	1
2	Multimeter	-	1

4.2 Components:

Sl. No.	Components	Specifications	Qty.
1	Resistors	10Ω,2Watt	1
2	MOSFET	IRF510	1
3	POT	5K	2

5. PROCEDURES:

Drain Characteristics:

1. Connections are made as per the circuit diagram.
2. Switch on the 230V AC supply.
3. Keep the gate - source voltage (V_{GS}) to a suitable value.
4. Now slowly increase the drain-source voltage (V_{DS}) by varying the pot till MOSFET get turned on, with the indication that drain-source voltage decreases to it on state voltage drops.
5. Note down the values of drain-source voltage (V_{DS}) and the drain current (I_D).
6. For various gate-source voltage take the different set of readings and tabulate it.
7. Finally, a graph of drain-source voltage (V_{DS}) Vs drain current (I_D) is plotted for various gate-source voltage.

Transfer Characteristics:

1. Connections are made as per the circuit diagram.
2. Switch on the 230V AC supply.
3. Keep the Drain - source voltage (V_{DS}) to a suitable value.
4. Now slowly increase the gate - source voltage (V_{GS}) by varying the pot till MOSFET get turned on, with the indication that drain current getting constant value.
5. Note down the values of gate-source voltage (V_{GS}) and the drain current(I_D).
6. Finally, a graph of gate - source voltage (V_{GS}) Vs drain current (I_D) is plotted.

6. EXPERIMENTAL DATA:

Table1

Data for Drain characteristics

V_{GS1}=		V_{GS2}=		V_{GS3}=	
V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)	V_{DS}(V)	I_D(mA)

Table2

Data for Transfer characteristics

V_{DS}=	
V_{GS}(V)	I_D(mA)

Result:

Parameters	Calculated Values
$r_D=\Delta V_{DS}/\Delta I_D$	
$g_m=\Delta I_D/\Delta V_{GS}$	
$\mu= r_D x g_m$	

7. DATA ANALYSIS:

(I) Plot the drain characteristics and transfer characteristics.
(II) Calculate MOSFET parameters from the graph.

8. PRECAUTIONARY MEASURE TO BE TAKEN:

1) Check the power supply terminals of the trainer kit.
2) Check the components to be used in the experiment.
3) Select proper mode of multimeter.
4) Connect the circuit carefully as per circuit diagram.
5) Don't give the power Supply without verifying the circuit by the class teacher.
6) The initial set gate voltage should be taken as minimum in order to take the consecutive readings.

9.SOME SAMPLE QUESTIONS:

i) What is current control device?
ii) What is voltage control device?
iii) What is the number and range of given MOSFET?
iv) Draw the symbol of MOSFET?
v) What is Transconductance?
vi) How to find the output resistance?

10. REFERENCE:

A. Electronics Laboratory Primer – A Design approach by S. Poorna Chandra & B Sasikala.
B. Linear Integrated Circuit by R.P. Jain & D. Roychowdhury.
C. Operational Amplifier and Linear Integrated Circuit by Ramakant A. Gayakwad.

Experiment no. 9

Title: Design, setup and plot the frequency response of Common Source JFET amplifier and obtain the bandwidth.

1. OBJECTIVE (S):

1.1 Design and implementation of a single stage JFET amplifier circuit using voltage divider biasing technique.

1.2. Determination of a) Mid band gain, b) Cut off frequencies, c) Bandwidth from frequency response curve.

2. THEORY:

In common source amplifier circuit Source terminal is made common to the other two terminals. In common source amplifier circuit input is applied between gate and source and output is taken between drain and source. The coupling capacitors are used to isolate D.C biasing from applied A.C signal from function generator and acts as short circuit for the A.C analysis. The high frequency characteristics of the FET amplifier are determined by the inter electrode and wiring capacitance.

Voltage divider bias Technique & graphical method:

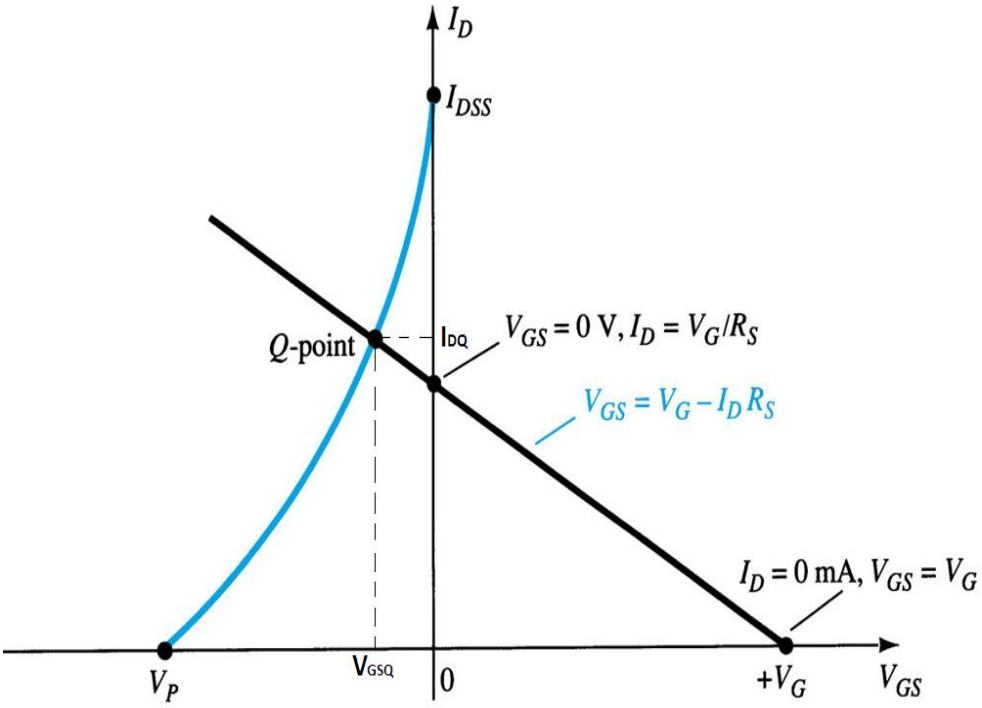
- The arrangement is the same as BJT but the DC analysis is different
- In BJT, I_B provide link to input and output circuit, in FET V_{GS} does the same.
- Taking I_G = 0A Kirchhoff's current law requires that I_{R1}= I_{R2} and to the left of the figure can be used to find the level of V_G.
- V_G can be found using the voltage divider rule :

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

- Using Kirchhoff's Law on the input loop:

$$V_G - V_{GS} - V_{RS} = 0$$
$$V_{GS} = V_G - I_D R_S$$

- Again the Q point needs to be established by plotting a line that intersects the transfer curve (Graphical Method).



1. Plot the line: By plotting two points: $V_{GS} = V_G$, $I_D = 0$ and $V_{GS} = 0$, $I_D = V_G/R_S$
2. Plot the transfer curve by plotting I_{DSS}, V_P and calculated values of I_D.
3. Where the line intersects the transfer curve is the Q point for the circuit.

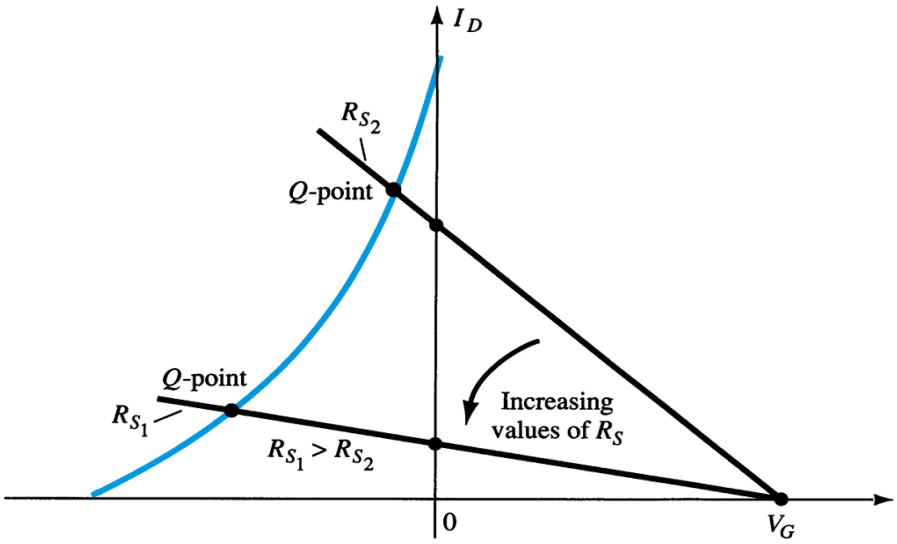
- Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be found.

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

- Output loop:

$$V_{DS} = V_{DD} - I_D(R_D + I_D R_S)$$
$$V_D = V_{DD} - I_D R_D$$
$$V_S = I_D R_S$$

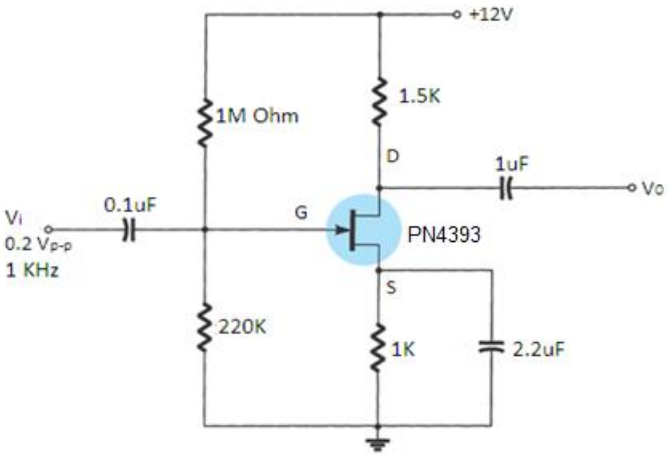
- Effect of increasing values of R_S



Capacitor calculations:

To provide low reactances almost short circuit at the operating frequency
f= 1KHz, $XC_S=0.1R_S$, $Xc_i=0.1R_{gs}$, $Xc_O=0.1R_D$
$C_S=1/(2\pi fXC_S)$, $Ci= 1/(2\pi fXC_1)$, $Co= 1/(2\pi fXC_2)$
But always higher values of capacitor are recommended. So thereby choosing appropriate value of R_1 , R_2 and R_S and fixing the Q point on trans-conductance curve (You have got in Exp No 5) using graphical method described above, we can easily design JFET amplifier.

3. CIRCUIT DIAGRAM:



4. APPARATUS & COMPONENTS USED:

4.1. Apparatus:

Sl. No.	Apparatus	Range	Qty.
1	Trainer Kit	-	1
2	CRO	20 MHz Bandwidth	1
3	Function Generator	0 MHz to 20 MHz	1
4	Multimeter	-	1

4.2. Components:

Sl. No.	Components	Specifications	Qty.
1	JFET	PN4393	1
2	Capacitor	0.1uF,1uF,2.2uF	1+1+1
4	Resistor	220K, ¼ Watt	1
5	Resistor	1.5K, ¼ Watt	1
6	Resistor	1K, ¼ Watt	1
7	Resistor	1 M Ohm, ¼ Watt	1

5. PROCEDURES:

Step1: Connect the circuit as per the circuit diagram.
Step2: Set V_i = 0.2V (p-p), 1KHz (say), using the Function generator.
Step3: Keeping the input voltage constant, vary the frequency from100Hz to 20MHz in logarithmic steps and note down the corresponding output voltage.
Step4: Note down the overall gain of the amplifier and calculate lower cut-off frequency, upper cut-off frequency and bandwidth.

6. EXPERIMENTAL DATA:

V_i = 0.2V (p-p)

Sl No.	Frequency	V_0 (volts)	Gain = V_0 / V_S	Gain (db) = 20 logV_0 / V_S

Result:

	Theoretical	Practical
Gain (Mid-band)		
Lower cut-off Frequency		
Upper cut-off Frequency		
Band width		

7. DATA ANALYSIS:

I. Plot the graph gain (dB) *vs.* frequency.
II. Calculate the bandwidth from the graph.

8. PRECAUTIONARY MEASURE TO BE TAKEN:

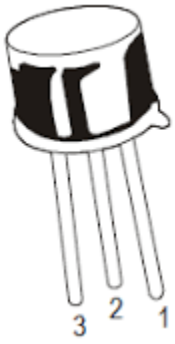
1) Check the power supply terminals of the trainer kit.
2) Check the components to be used in the experiment.
3) Select proper mode of multimeter.
4) Connect the circuit carefully as per circuit diagram.
5) Don't switch on the power Supply without verifying the circuit by the class teacher.
6) Applied voltage and current should not exceed the maximum ratings of the given transistor.

9. SOME SAMPLE QUESTIONS:

(i) What is meant transconductance with respect to JFET?
(ii) What are the characteristics of CS amplifier?
(iii) Define: lower cut-off frequency, upper cut-off frequency, mid-band frequency, centre frequency and band-width.
(iv) Define operating point and amplification factor.

10. REFERENCE:

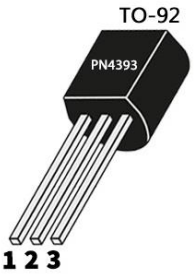
(A) Electronics Devices and circuit Theory- Boylestad & Nashelsky
(B) Electronics Principles-Malvino

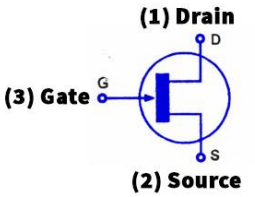


CL100

PIN CONFIGURATION
1. EMITTER
2. BASE
3. COLLECTOR

PN4393 Pinout





IRF510 Pinout